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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/918,734	07/31/2001	Rajiv Jain	10010445-1	2707

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AGILENT TECHNOLOGIES, INC.
Legal Department, DL429
Intellectual Property Administration
P.O. Box 7599
Loveland, CO 80537-0599

EXAMINER	
GUILL, RUSSELL L	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 03/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/918,734	JAIN ET AL.	
	Examiner	Art Unit	
	Russell L. Guill	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/31/2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 1 pg
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 14 have been examined. Claims 1 – 14 have been rejected.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1 and 8 are rejected under 35 U.S.C. 112, second paragraph, for use of an improper Markush group. Claims 1 and 8 recite the limitation "at least one attribute selected from a group comprising an AND attribute and an XOR attribute". This constitutes an improper Markush group. The MPEP Section 2173.05(h) Section I. Alternative Limitations recites:

> Alternative expressions are permitted if they present no uncertainty or ambiguity with respect to the question of scope or clarity of the claims. One acceptable form of alternative expression, which is commonly referred to as a Markush group, recites members as being "selected from the group consisting of A, B and C." See Ex parte Markush, 1925 C.D. 126 (Comm'r Pat. 1925).
>
> Ex parte Markush sanctions claiming a genus expressed as a group consisting of certain specified materials. Inventions in metallurgy, refractories, ceramics, pharmacy, pharmacology and biology are most frequently claimed under the Markush formula but purely mechanical features or process steps may also be claimed by using the Markush style of claiming. See Ex parte Head, 214 USPQ 551 (Bd. App. 1981); In re Gaubert, 524 F.2d 1222, 187 USPQ 664 (CCPA 1975); and In re Harnisch, 631 F.2d 716, 206 USPQ 300 (CCPA 1980). ***It is improper to use the term "comprising" instead of "consisting of."*** Ex parte Dotter, 12 USPQ 382 (Bd. App. 1931).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dave (U.S. Patent Number 6,289,488), in view of Markov (U.S. Patent Number 6,305,006 B1), and further in view of Kalavade (Kalavade, Asawaree, and Subrahmanyam, P. A.; "Hardware/Software Partitioning for Multifunction Systems", September 1998, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems).

5.1. The art of Dave is directed to hardware/software co-synthesis of system-level architecture for embedded systems (Abstract, lines 1 – 5).

5.2. Dave teaches forming an initial master task graph from a specification (column 2, lines 60 – 62, and column 3, lines 9 – 13), said initial master task graph including at least one hierarchical task having pointers to a plurality of sub-task graphs (figures 2A, 2B, and 2C; column 5, lines 55 – 65), and at least one attribute

selected from a group comprising an AND attribute and an XOR attribute (figure 2A).

5.2.1. Regarding figure 2A; the dependent tasks t2 and t4 obviously have an AND attribute.

5.3. Dave further teaches processing the initial master task graph to provide a selected number of final master task graphs, each of said final master task graphs comprising a list of AND task graphs (figure 2C, and column 14, lines 47 – 65).

5.4. Dave does not teach forming an initial master task graph from **multiple specifications**, said initial master task graph including at least one hierarchical task having pointers to a plurality of sub-task graphs, and at least one attribute selected from a group comprising an AND attribute and an XOR attribute.

5.5. Dave further does not teach generating a family of architectures for each of said final master task graphs, each of the architectures generated for a given final master task graph being capable of executing every AND task graph included in the list for the given final master task graph.

5.6. Dave further does not teach exploring each of said generated architectures for use in executing said multiple specifications.

5.7. The art of Markov is directed to generating candidate architectures for an architectural exploration based electronic design creation process (Title of patent).

5.8. Markov teaches generating a family of architectures for each of said final master task graphs, each of the architectures generated for a given final master task graph being capable of executing every AND task graph included in the list for the given final master task graph (figure 1, and column 2, lines 19 – 25).

5.9. Markov further teaches exploring each of said generated architecture for use in executing said specification (figure 1, items 104, 102, and 106, column 4, lines 46 – 62).

5.10. Regarding claim 8, Markov further teaches a computer readable medium and executable instructions stored thereon (column 20, lines 10-16).

5.11. The art of Kalavade is directed to multifunction systems and system-level design (page 819, left column, section Index Terms)

5.12. Kalavade teaches multiple specifications for systems (page 819, section Introduction).

5.13. The arts of Dave, Markov, and Kalavade are analogous art because they all are directed to the problem of synthesis of electronic systems.

5.14. The motivation for combining the art of Markov with the art of Dave would have been obvious in view of the suggestion in Markov of the benefit of exploring multiple architectures (Markov, column 1, lines 56 – 63). The ordinary artisan at the time of invention

would have been motivated to search the prior art in order to benefit from the inventions of others.

5.15. The motivation for combining the art of Kalavade with the art of Dave would have been obvious in view the suggestion in Kalavade of the benefit of optimizing the system design for multifunction systems (Kalavade, page 819, section Abstract). The ordinary artisan at the time of invention would have been motivated to search the prior art in order to benefit from the inventions of others.

5.16. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Markov and the art of Kalavade with the art of Dave for the benefit of obtaining the invention specified in claims 1 and 8.

6. Claims 2 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dave (U.S. Patent Number 6,289,488), and Markov (U.S. Patent Number 6,305,006 B1), and Kalavade (Kalavade, Asawaree, and Subrahmanyam, P. A.; "Hardware/Software Partitioning for Multifunction Systems", September 1998, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems), in view of Wolf (Wolf, W., Xie, Y.; "Allocation and scheduling of conditional task graph in hardware/software co-synthesis", March 2001, Proceedings of the conference on Design, Automation and Test in Europe).

6.1. Claim 2 is a dependent claim of claim 1 and thereby inherits all the rejected limitations of claim 1.

6.2. Claim 9 is a dependent claim of claim 8 and thereby inherits all the rejected limitations of claim 8.

6.3. Dave does not teach an initial master task graph that includes a first hierarchical task having an AND attribute, and a second hierarchical **task having an XOR attribute**.

6.4. The art of Wolf is directed to hardware/software co-synthesis of system-level architecture for embedded systems (Abstract, lines 1 – 5).

6.5. Wolf teaches a task graph having an XOR attribute (page 621, figure 1, and right-side column, lines 1 – 5).

6.5.1. Regarding (page 621, figure 1, and right-side column, lines 1 – 5); it is obvious that a conditional branch is the same as an XOR attribute.

6.6. The art of Wolf and the art of Dave are analogous art because they are both directed to the problem of hardware/software co-synthesis of system-level architecture.

6.7. The motivation for combining the art of Kalavade with the art of Dave would have been obvious in view the suggestion in Kalavade of the benefit of optimizing the system design for multifunction systems (Kalavade, page 819, section Abstract). The ordinary artisan at the time of invention would have been motivated to

search the prior art in order to benefit from the prior inventions of others.

6.8. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Wolf with the art of Dave for the benefit of obtaining the invention specified in claims 2 and 9.

7. Claims 3 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dave (U.S. Patent Number 6,289,488), and Markov (U.S. Patent Number 6,305,006 B1), and Kalavade (Kalavade, Asawaree, and Subrahmanyam, P. A.; "Hardware/Software Partitioning for Multifunction Systems", September 1998, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems) and Wolf (Wolf, W., Xie, Y.; "Allocation and scheduling of conditional task graph in hardware/software co-synthesis", March 2001, Proceedings of the conference on Design, Automation and Test in Europe).

7.1. Claim 3 is a dependent claim of claim 2 and thereby inherits all the rejected limitations of claim 2.

7.2. Claim 10 is a dependent claim of claim 9 and thereby inherits all the rejected limitations of claim 9.

7.3. Dave teaches to resolve the initial master task graph into sets of AND task graphs on the basis of respective sub-task graphs

associated with the first hierarchical task (figures 2A, 2B, and 2C); and resolving sets of AND task graphs into final master task graphs (figures 2A, 2B, and 2C).

8. Claims 4 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dave (U.S. Patent Number 6,289,488), and Markov (U.S. Patent Number 6,305,006 B1), and Kalavade (Kalavade, Asawaree, and Subrahmanyam, P. A.; "Hardware/Software Partitioning for Multifunction Systems", September 1998, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems).

8.1. Claim 4 is a dependent claim of claim 1 and thereby inherits all the rejected limitations of claim 1.

8.2. Claim 11 is a dependent claim of claim 8 and thereby inherits all the rejected limitations of claim 8.

8.3. Markov teaches that a final master task graph is applied to an architecture synthesis engine to generate a family of architectures therefor (Abstract, and figure 1, items 108, 102, 106, and column 2, lines 20-27).

9. Claims 5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dave (U.S. Patent Number 6,289,488), and Markov (U.S. Patent Number 6,305,006 B1), and Kalavade (Kalavade, Asawaree, and Subrahmanyam, P. A.; "Hardware/Software Partitioning for Multifunction Systems", September 1998, IEEE

Transactions on Computer-Aided Design of Integrated Circuits and Systems) in view of Dick (Dick, Robert P., and Jha, Niraj K.; "MOGAC: A Multiobjective Genetic Algorithm for the Co-Synthesis of Hardware-Software Embedded Systems", 1997,Digest of Technical Papers, 1997 IEEE/ACM International Conference on Computer-Aided Design, 9-13 November 1997).

9.1. Claim 5 is a dependent claim of claim 1 and thereby inherits all the rejected limitations of claim 1.

9.2. Claim 12 is a dependent claim of claim 8 and thereby inherits all the rejected limitations of claim 8.

9.3. The art of Dick is directed to hardware/software co-synthesis of system-level architecture.

9.4. Dave does not teach placing each of the architectures generated for a given final master task graph into a pool; and retaining a particular architecture in said pool only if said particular architecture can execute each AND task graph of said given final master task graph in accordance with a prespecified time schedule.

9.5. Dick teaches placing each of the architectures generated for a given final master task graph into a pool (section 2.2 Genetic Algorithms, lines 1-5, and section 3.1 Overview of the Algorithm, and section 3.7 Performance Evaluation, subsection Cost calculation, and subsection Constraint Violation); and retaining a

particular architecture in said pool only if said particular architecture can execute each AND task graph of said given final master task graph in accordance with a prespecified time schedule (section 2.2 Genetic Algorithms, lines 1-5, and section 3.1 Overview of the Algorithm, and section 3.7 Performance Evaluation, subsection Cost calculation, and subsection Constraint Violation).

9.6. The art of Dick and the art of Dave are analogous art because they are both directed to the problem of hardware/software co-synthesis of system-level architecture.

9.7. It was common knowledge to the ordinary artisan at the time of invention to use genetic algorithms for the synthesis of architecture (Dick, entire document).

9.8. The motivation for combining the art of Dick with the art of Dave would have been the expectation of benefit to overcome the limitations expressed in Dave of architectures that are either over-designed or fail to meet constraints, and the suggestion to use design automation (Dave, column 1, lines 39-48). The ordinary artisan would have been motivated to search the prior art in order to benefit from prior art methods.

9.9. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Dick

with the art of Dave for the benefit of obtaining the inventions specified in claims 5 and 12.

10. Claims 6 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dave (U.S. Patent Number 6,289,488), in view of Markov (U.S. Patent Number 6,305,006 B1), and Kalavade (Kalavade, Asawaree, and Subrahmanyam, P. A.; "Hardware/Software Partitioning for Multifunction Systems", September 1998, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems).

10.1. Claim 6 is a dependent claim of claim 1 and thereby inherits all the rejected limitations of claim 1.

10.2. Claim 13 is a dependent claim of claim 8 and thereby inherits all the rejected limitations of claim 8.

10.3. Dave does not teach that a generated architecture is disposed to execute specified multiple tasks from task specifications on a single component that is selected from the set of resources.

10.4. Kalavade teaches that a generated architecture is disposed to execute specified multiple tasks from task specifications on a single component that is selected from the set of resources (page 834, tableIV, applications M2E and H share resource HA1).

11. Claims 7 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dave (U.S. Patent Number 6,289,488), in view of Markov (U.S. Patent Number 6,305,006 B1), and Kalavade (Kalavade,

Asawaree, and Subrahmanyam, P. A.; "Hardware/Software Partitioning for Multifunction Systems", September 1998, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems).

11.1. Claim 7 is a dependent claim of claim 1 and thereby inherits all the rejected limitations of claim 1.

11.2. Claim 14 is a dependent claim of claim 8 and thereby inherits all the rejected limitations of claim 8.

11.3. Dave does not teach that a generated architecture is disposed to execute specified multiple tasks from task specifications on the same type, but different instances, of a component that is selected from the set of resources.

11.4. Kalavade teaches that a generated architecture is disposed to execute specified multiple tasks from task specifications on the same type, but different instances, of a component that is selected from the set of resources (page 834, tableIV, application M2E uses a resource CP and application H uses two resources CP).

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russell L. Guill whose telephone number is 571-272-7955. The examiner can normally be reached on Monday - Friday 9:00 AM – 5:30 PM.

13. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 571-272-3716. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RLG

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER